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10/551,802	12/02/2005	Satoshi Sugahara	125471	6737

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EXAMINER	
VALENTINE, JAMI M	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/551,802	SUGAHARA ET AL.	
	Examiner	Art Unit	
	Jami M. Valentine, Ph.D.	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-99* is/are pending in the application.

4a) Of the above claim(s) *1-34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *35-99* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/30/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of the Application

1. **Claims 1-99** are pending in this application.

Election/Restrictions

2. Applicant's election of **Group 6 (Claims 35-99)** in the reply filed on 4/23/2007 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). The requirement is still deemed proper and is therefore made FINAL.

3. **Claims 1-34** are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

4. **Claims 35-99** are examined in this Office action.

US National Phase of PCT

5. Acknowledgment is made that this application is the US national phase of international application PCT/JP04/04512 filed 30 March 2004 which designated the U.S. and claims benefit of JP 2003-095600, filed 31 March 2003.

Foreign Priority

6. Acknowledgment is made that the certified copy of the foreign priority document has been received in the national stage application from the International Bureau.

Information Disclosure Statement

7. Acknowledgment is made that the information disclosure statement has been received and considered by the examiner. If the applicant is aware of any prior art or any other co-

pending applications not already of record, he/she is reminded of his/her duty under 37 CFR 1.56 to disclose the same.

Drawings

8. The drawings are objected to because figures 9, 10, 11A-11D, 12A-12D, 13A-13D, 14A-14D, 15A-15C, 16A-16C and 17 are informal. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

9. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "concave portion" from claim 62 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing

sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

10. Figure 8 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

11. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the

following is required: claim 62 recites a **"concave portion"** of the substrate, however, there is no mention of a concave portion in the specification.

12. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

13. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

14. **Claims 37-38, 40, 42-43, 47-49, 56, 63-76, and 99** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

15. Per **Claims 37 and 42, 47-48, 63-72**, the following language is indefinite: " ...the ferromagnetic source..." The claims from which these claims depend do not recite a ferromagnetic source. Hence, there is insufficient antecedent basis for this limitation in the claims.

16. Per **Claims 38 and 43, 47-48, 63-72**, the following language is indefinite: " ...the ferromagnetic drain ..." The claims from which these claims depend do not recite a ferromagnetic drain. Hence, there is insufficient antecedent basis for this limitation in the claims.

17. Per **Claims 40, 63-68,** the following language is indefinite: " ... the non-magnetic tunnel barrier ..." The claims from which these claims depend do not recite a non-magnetic tunnel barrier. Hence, there is insufficient antecedent basis for this limitation in the claims.

18. Per **Claims 47 , 49, 63-67**, the following language is indefinite: " ... the ferromagnetic electrode..." The claims from which these claims depend do not recite a ferromagnetic electrode. Hence, there is insufficient antecedent basis for this limitation in the claims.

19. Per **Claim 50** the following language is indefinite: "...the ferromagnetic electrode is a half-metal ferromagnetic material, the non-magnetic tunnel barrier or the ferromagnetic tunnel barrier..." Claim 50 depends on claim 35, but claim 35 does not recite any of the following: a ferromagnetic electrode, a non-magnetic tunnel barrier or a ferromagnetic tunnel barrier. Hence, there is insufficient antecedent basis for this limitation in the claims.

20. Per **Claim 56**, the following language is indefinite: " ... the ferromagnetic electrode or the non-magnetic electrode is separated from the ferromagnetic semiconductor layer and the substrate by the non-magnetic tunnel barrier or the ferromagnetic tunnel barrier ..." Claim 56 depends on claims 54 and 35, however claims 54 and 5 do not recite any of the following: a ferromagnetic electrode, a non-magnetic electrode, a non-magnetic tunnel barrier or a ferromagnetic tunnel barrier . Hence, there is insufficient antecedent basis for this limitation in the claims.

21. Per **Claim 68**, the following language is indefinite: " ... the non-magnetic source..." Claim 49 depends on claim 35, however claim 35 does not recite a non-magnetic source. Hence, there is insufficient antecedent basis for this limitation in the claims

22. Per **Claim 99**, the following language is indefinite: " ... the word line ..." The claims from which these claims depend do not recite a word line Hence, there is insufficient antecedent basis for this limitation in the claims.

23. The examiner has found 44 instances non-compliance with the second paragraph of 35 USC § 112. That Applicant has bothered to ensure that the claim language complies with the law has exerted a serious burden on the examiner.

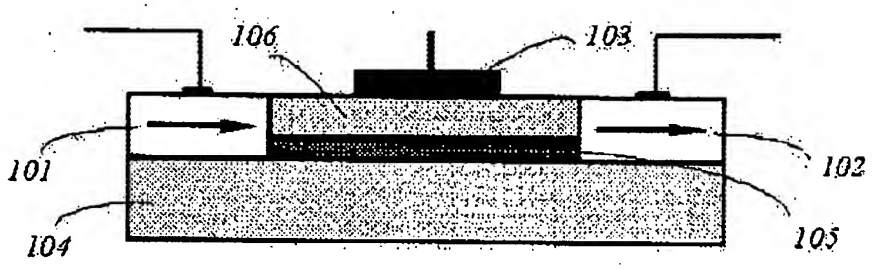
Claim Rejections - 35 USC § 102

24. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

25. Insofar as definite, the claims are interpreted for examination in view of the existing prior art as follows: **Claims 35, 37-38, 40-51, 53-57, 61 and 63-76** are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al. (US Patent Application Publication No 2004/0041217) hereinafter referred to as Lee.

26. Per **Claim 35** Lee discloses a transistor, comprising a ferromagnetic semiconductor layer, a source (101) that injects carriers into the ferromagnetic semiconductor layer; and a drain (102) that receives the carriers injected into the ferromagnetic semiconductor layer a gate electrode (103) that applies a voltage for controlling conduction of the carriers from the source to the drain [0059]. Lee [0058] teaches that the ferromagnetic semiconductor material can be changed to have a ferromagnetic property or to have a non-ferromagnetic property by controlling a carrier concentration with a gate voltage. With this understanding, the device of Lee discloses combinations of ferromagnetic and/or non-ferromagnetic sources and drains.



Prior Art: Lee Figure 11

27. Per **Claims 37 and 42** Lee discloses the transistor of claim 35, including where when the source is the ferromagnetic source, the drain is a non-magnetic drain that comprises a non-magnetic tunnel barrier (106) joined to the ferromagnetic semiconductor layer, and a non-magnetic electrode (103) joined to the non-magnetic tunnel barrier .

28. Per **Claims 38 and 43** Lee discloses the transistor of claim 35, including where when the drain is the ferromagnetic drain, the source is a non-magnetic source that comprises a non-magnetic tunnel barrier (106) joined to the ferromagnetic semiconductor layer, and a non-magnetic electrode (103) joined to the non-magnetic tunnel barrier .

29. With regard to **claims 37 – 38 and 42 - 43**, these limitations are **"product-by-process"** limitations describing intermediate structures. A "product by process" claim limitation is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17(footnote 3). See also in re Brown, 173 USPQ 685: In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324: In re Avery, 186 USPQ 116 in re Wertheim, 191 USPQ 90 (209 USPQ 254 does not deal with this issue); and In re Marosi et al, 218 USPQ 289 final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by process" claims or

not. Note that Applicant has the burden of proof in such cases, as the above case law makes clear.

30. Per **Claim 40** Lee discloses the transistor of claim 35, including where the non-magnetic tunnel barrier (106) is made of a semiconductor that is the base material of the ferromagnetic semiconductor layer. [0059]

31. Per **Claim 41** Lee discloses the transistor of claim 35, including where one of the source and the drain is a ferromagnetic source (101) or a ferromagnetic drain (102) that comprises a ferromagnetic tunnel barrier (106) joined to the ferromagnetic semiconductor layer (105), and a non-magnetic electrode (103) joined to the ferromagnetic tunnel barrier .

32. Per **Claim 44** Lee discloses the transistor of claim 35, including where the source (101) and the drain are a ferromagnetic source (101) and a ferromagnetic drain (102) each comprising a ferromagnetic tunnel barrier (106) joined to the ferromagnetic semiconductor layer, and a non-magnetic electrode (103) joined to the ferromagnetic tunnel barrier .

33. **Claim 45** recites the energetic performance properties of the device depending on the carrier type. This **functional limitation** does not distinguish the claimed device over the prior art, since it appears that this limitation can be performed by the prior art structure of Lee. While features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429,1431-32 (Fed. Cir. 1997) See MPEP 2114.

34. Per **Claim 46** Lee discloses the transistor of claim 35, including where the ferromagnetic semiconductor layer is formed with a ferromagnetic semiconductor having magnetic elements

added to a semiconductor. [0028] The limitations of claim 46 are "product-by-process" limitations. See the above discussion regarding product by process limitations.

35. Per **Claim 47** Lee discloses the transistor of claim 35, including where the ferromagnetic source (101) or the ferromagnetic drain (102) comprises the ferromagnetic electrode that is a ferromagnetic semiconductor. (see above discussion)

36. Per **Claim 48** Lee discloses the transistor of claim 35, including where the ferromagnetic source (101) or the ferromagnetic drain (102) includes an insulating ferromagnetic material as the ferromagnetic tunnel barrier (105). [0058-0059]

37. **Claim 48** recites the energetic performance properties of the device depending on the carrier type. This functional limitation does not distinguish the claimed device over the prior art, since it appears that this limitation can be performed by the prior art structure of Lee. See the above discussion regarding functional limitations.

38. Per **Claim 49** Lee discloses the transistor of claim 35, including where the ferromagnetic semiconductor employed for the ferromagnetic electrode is a ferromagnetic semiconductor having magnetic elements added to a semiconductor. [0028]

39. With regard to **claim 50**, this limitation is a "product-by-process" limitation describing an intermediate structure. See the above discussion regarding product by process limitations.

40. Further **Claim 50** recites the performance properties of the device. This functional limitation does not distinguish the claimed device over the prior art, since it appears that this limitation can be performed by the prior art structure of Lee. See the above discussion regarding functional limitations.

41. Per **Claim 51** Lee discloses the transistor of claim 35, including where an insulating layer (106) is interposed between the gate electrode (103) and the ferromagnetic semiconductor layer (105).

42. Per **Claim 53** Lee discloses the transistor of claim 51, including where the insulating layer is grown or deposited on the ferromagnetic semiconductor layer. The limitations of claim 53 are "product-by-process" limitations. See the above discussion regarding product by process limitations.

43. Per **Claim 54** Lee discloses the transistor of claim 35, including where the transistor is formed on a substrate having an insulating layer formed thereon. [0060]

44. Per **Claims 55 and 57** Lee discloses the transistor of claim 54, including where the transistor is formed on the substrate; the junction interface of the source and the drain in the vicinity of the gate electrode is substantially perpendicular to the principal surface of the substrate; and the flowing direction of the carriers moving from the source to the drain is in a plane substantially parallel to the principal surface of the substrate. (As shown in figure 11)

45. Per **Claim 56** Lee discloses the transistor of claim 54, including where the electrode (103) is separated from the ferromagnetic semiconductor layer (105) and the substrate (104) by the tunnel barrier (106).

46. Per **Claim 61** Lee discloses the transistor of claim 54, including where the transistor is formed on the substrate; the junction interface of the source and the drain with the ferromagnetic semiconductor in the vicinity of the gate electrode is substantially parallel to the principal surface of the substrate; and the flowing direction of the carriers moving from the source to the drain is in a plane substantially parallel to the principal surface of the substrate. (see figure 11)

47. Per **Claim 63 –76** Lee discloses the transistor of claims 35 and 54. These limitations are "functional limitations". See the above discussion regarding functional limitations.

Claim Rejections - 35 USC § 103

48. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

49. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

50. **Claims 36, 39, 52 and 62** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee.

51. Per **Claim 36** Lee discloses the transistor of claim 35, including where one of the source and the drain is a ferromagnetic source (101) or a ferromagnetic drain (102) that comprises a non-magnetic tunnel barrier (106) that is joined to the ferromagnetic semiconductor layer, and an electrode joined to the non-magnetic tunnel barrier but fails to teach where the electrode is a ferromagnetic electrode.

52. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the electrode from a ferromagnetic material since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for its intended use as a matter of design choice. *In re Leshin,* 125 USPQ 416.

53. Per **Claim 39** Lee discloses the transistor of claim 35, including where the source (101) and the drain (102) each comprise a non-magnetic tunnel barrier (106) joined to the ferromagnetic semiconductor layer (105), and an electrode (103) joined to the non-magnetic tunnel barrier (106) but fails to teach where the electrode is a ferromagnetic electrode.

54. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the electrode from a ferromagnetic material since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for its intended use as a matter of design choice. *In re Leshin,* 125 USPQ 416.

55. Per **Claim 52** Lee discloses the transistor of claim 51, including an insulating layer but fails to teach where the insulating layer comprises a surface oxide layer.

56. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the insulating layer from a surface oxide layer since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for its intended use as a matter of design choice. *In re Leshin,* 125 USPQ 416.

57. Additionally, **Claim 52** contains product by process limitations. See the above discussion regarding product by process limitations.

58. Per **Claim 62**, Lee teaches the transistor of claim 61 as well as a structure in which a ferromagnetic semiconductor layer (105), a ferromagnetic tunnel barrier (106), and a non-magnetic electrode (103) are stacked in this order on the substrate;

59. Lee fails to teach a concave portion is formed in the substrate, the concave portion having a bottom with such a depth as to reach the ferromagnetic semiconductor layer or the inside of the ferromagnetic magnetic semiconductor layer; and a gate insulating film and a gate electrode are formed on the inner surface of the concave portion.

60. It would have been obvious as a matter of design choice to one having ordinary skill in the art at the time the invention was made to form the device of lee on a "concave" portion of the substrate since applicant has not disclosed that to do so solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with the flat substrate of Lee.

61. **Claims 58-60** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Burns Jr. et al. (US Patent No 5,874,760), hereinafter referred to as Burns

62. Per **Claims 58-60** Lee teaches the device of claim 54 including a source, a ferromagnetic semiconductor, and a drain.

63. Lee fails to teach where the source, ferromagnetic semiconductor and drain are stacked substantially in parallel with the principal surface of the substrate; and a gate insulating film and a gate electrode that are formed on a side surface of the stacked structure.

64. Burns teaches a memory device where the source, ferromagnetic semiconductor and drain are stacked substantially in parallel with the principal surface of the substrate; and a gate insulating film and a gate electrode that are formed on a side surface of the stacked structure, and

where a conductive semiconductor layer formed on the substrate serves as a contact layer for the source. (see Figure 10)

65. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the device of Lee with the device of Burns, in order to reduce size and power consumption of the chip, and allow faster operation (Burns column 1 lines 37-54)

66. **Claims 77-84, 86-93 and 95-98** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Kuroda et al. (US Patent No 5,457,335), hereinafter referred to as Kuroda.

67. Per **Claim** 77, Lee discloses the transistor of claim 35 but fails to teach; a first line that is connected to the gate electrode; a second line that is connected to the drain: and a third line that grounds the source.

68. Kuroda teaches a memory element where the control gate of the memory element is connected with the word line, the drain is connected with the data line, and the source is connected with the ground line. (column 10 lines 38-45). This circuit is makes the device erasable (an information re-write unit) see column 25 line 57 through column 26 line 5.

69. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the device of Lee with the device of Kuroda in order to use the improved memory structure of Lee in what was a conventional circuit (that of Kuroda) at the time the invention was made. These types of line circuits were common knowledge in the art at the time of Applicant's invention.

70. Per **Claim 78-81** Lee in view of Kuroda discloses the memory element of claim 77. These limitations are "functional limitations". These functional limitations do not distinguish the

claimed device over the prior art, since it appears that each of these limitations can be performed by the prior art structure of Lee in view of Kuroda. See the above discussion regarding functional limitations.

71. Per **Claims 82-84 and 90-93** Lee discloses the transistor of claim 35 but fails to teach: a ground line that collectively grounds the sources of a first group of transistors that are selected from the transistors; a word line that are collectively connected to the gates of the first group of transistors; and a bit line that are connected to the drains of the first group of transistors independently of one another, and are also collectively connected to a second group of transistors including transistors that do not belong to the first group.

72. Kuroda teaches a memory element where the control gate of the memory element is connected with the word line, the drain is connected with the data (bit) line, and the source is connected with the ground line. (column 10 lines 38-45). This circuit is makes the device erasable (an information re-write unit) see column 25 line 57 through column 26 line 5.

73. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the device of Lee with the device of Kuroda in order to use the improved memory structure of Lee in what was a conventional circuit (that of Kuroda) at the time the invention was made. These types of line circuits were common knowledge in the art at the time of Applicant's invention. Further it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 103 USPQ 8.

74. Per **Claim 86-89, and 95-98:** These limitations are "functional limitations". These functional limitations do not distinguish the claimed device over the prior art, since it appears

that each of these limitations can be performed by the prior art structure of Lee in view of Kuroda. See the above discussion regarding functional limitations.

75. **Claims 85 and 94** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Kuroda further in view of Nakajima et al. (US Patent Application Publication No 2002/0006058), hereinafter referred to as Nakajima

76. **Per Claims 85 and 94** Lee in view of Kuroda teaches the device of claim 35 including transistors as in claim 35 adjacent to each other, a word line that is respectively connected to the gate electrode of the first transistor and the gate electrode of the second transistor; a first bit line that is connected to the drain of the first transistor; a second bit line that is connected to the drain of the second transistor;

77. Lee in view of Kuroda fails to teach a source that is shared between the first and second transistors; and a line that grounds the shared source, and extends in a direction perpendicular to the bit lines.

78. Nakajima teaches a magnetic memory device with a source that is shared between the first and second transistors [0202]; and a line that grounds the shared source, and extends in a direction perpendicular to the bit lines. (grounded bit line [0024]).

79. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the device of Lee in view of Kuroda with the device of Huffman, in order to reduce the device size. (Nakajima [0202])

80. **Claim 99** is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Kuroda further in view of Chen et al. (US Patent No 5,659,499), hereinafter referred to as Chen

81. **Per Claim 99** Lee in view of Kuroda teach the device of claim 77 but fails to teach a yoke that surrounds the outer periphery of the first line.

82. Chen teaches a memory device including a yoke (material (17)) that surrounds the outer periphery of the first line (column 2 lines 9-26, also see, claim 12, the yoke layer lies above the metal layer.) Those skilled in the magnetic memory arts define a yoke as a thin film comprising high magnetic permeability material is provided around a writing wire (for example, refer to [0009] of US PAP No 2004/0141367 is provided as a teaching reference).

83. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the device of Lee in view of Kuroda with the device of Huffman, in order to provide a device that where the magnetic fields are concentrated at the memory elements. (Chen column 2 lines 24-26)

Cited Prior Art

84. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Reference 1: US Patent Application Publication No 2004/0141367 by Amano et al.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jami M. Valentine, Ph.D. whose telephone number is (571) 272-9786. The examiner can normally be reached on Mon-Thurs 8:30am-7pm EST. **NOTE**: From June 18 through August 8th, The examiner will be available *only* on Thursdays and Fridays 8:30am-7pm EDT, due to jury duty service.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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